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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
KAWSAR, ABDULLAH AL	

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2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,335	KIMELMAN ET AL.	
	Examiner	Art Unit	
	ABDULLAH AL KAWSAR	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/22/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/01/2008 has been entered.

Information Disclosure Statement

3. The information disclosure statement filed on 12/22/2008 with reference under "other Documents" the reference "Japanese official action mailed December 9, 2008 in corresponding Japanese Application No. 2004-367705" has not been considered by the examiner because the reference was not in English and there wasn't any translation provided to understand the document to its merits.

Specification

4. The abstract of the disclosure is objected to because a deletion of "[Figure 7]" in line 10 is required. Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claim 1 objected to because of the following informalities: claim 1 line recites "store" and line 7 recites "saving", applicant is suggested to use the same terminology throughout the claim for reciting the same step or element. Appropriate correction is required.

6. Claims 5 and 18 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 5 and 18 have limitation already disclosed in independent claims 1 and 14 accordingly.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following claims languages are not clearly understood:

i. As per claim 1, line 18-19 recites "determine stack priority level" it is unclear why stack priority level is being determined as there is no date stored in the stack after the process has been reloaded as recited in line 16, it is also not clear what is the difference between the stack priority level and the interrupted

process priority level as there is only one set of data in the stack at any time. The relationship between "the stack priority level", "Interrupt event priority" and "processing priority" is not clear and it is also not clear if the waiting interrupts and the interrupted process are saved in the same stack or being saved in different table or stack. Line 21-24 it is unclear why the detecting step is done as it is redundant as the detecting has already been done in line 10-12 and moreover there are no data left in the stack as the interrupted process has already been reloaded in line 16-18 after the initial detection in line 10-12. Line 20 recites "one or more sets of data" it is unclear how can stack have more than one set of data at any time as the there only one process interrupted to service an interrupt routine and that interrupt event is not interrupted or pre-empted until that interrupt event is complete as recited in line 10.

ii. Claim 14 has similar deficiency as claim 1 above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-7, 10-12, 14-20 and 23-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Miu et al.(Miu) US Patent No. 4,488,227, in view of Ishimoto et al.(Ishimoto) US Patent No. 5,410,715.

11. As per claim 1, Miu teaches the invention substantially as claim including Apparatus for processing data (col 1, lines 9-12), said apparatus comprising:

processing configured to perform processing operations under control of program instructions(col 4, lines 14-19); and

a stack data store configured to store one or more sets of state data, each set associated with a respective processing performed by said processor when an interrupt event occurs, (col 4, lines 11-22);

an interrupt controller(col 4, lines 22-24), in response to a first interrupt event, for saving to a stack data store first state data associated with processing being performed when said first interrupt event occurred and for redirecting program instruction execution to a first interrupt handling program (col 4, lines 15-30) and

(i) if said one or more second interrupt events has occurred, then redirecting program instruction execution to a second interrupt handling program without saving(neither pushed nor popped) further state data to said stack data store(abstract lines 10-17 and col 4 lines 36-43); and

(ii) if said one or more second interrupt event has not occurred, then reloading said first state data from said stack data store and to resume said processing that was interrupted by said first interrupt event (col 3 lines 4-12).

Miu does not specifically disclose each interrupt is associated with a programmable priority level; that upon completion of said first interrupt handling program, for detecting if one or more second interrupt events having a higher priority than said processing that was interrupted

by said first interrupt event has occurred during execution of said first interrupt handling program; wherein said interrupt controller is further configured to determine a stack priority level corresponding to highest priority interrupt event among the interrupt events associated with said one or more sets of state data stored in said stack data store; and said interrupt controller is further configured to detect that said one or more second interrupt events have a higher priority than said processing that was interrupted by said first interrupt event if one or more second interrupt event has a higher priority than said stack priority level.

However, Ishimoto discloses each interrupt is associated with a programmable priority level (col 4, lines 61-64);

that upon completion of said first interrupt handling program, for detecting if one or more second interrupt events having a higher priority than said processing that was interrupted by said first interrupt event has occurred during execution of said first interrupt handling program (col 4, lines 4-12, lines 16-34);

wherein said interrupt controller is further configured to determine a stack priority level corresponding to highest priority interrupt event among the interrupt events associated with said one or more sets of state data stored in said stack data store (col 1, lines 24-40); and

said interrupt controller is further configured to detect that said one or more second interrupt events have a higher priority than said processing that was interrupted by said first interrupt event if one or more second interrupt event has a higher priority than said stack priority level (col 4, lines 65-68 through col 5, lines 1-21).

12. Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Ishimoto into the method of Miu for detecting one or more higher priority interrupt during the execution of the first interrupt. The modification would have been obvious because one of the ordinary skills of the art would want to detect the higher priority level interrupts for execution for better interrupt handling and control.

13. As per claim 2, Miu teaches wherein said first state data includes one or more of: a program counter value corresponding a current program execution point (figure 5, sheet 1 element 63, 66, and 64);

a processor status register value corresponding one or more state variables of said apparatus (col 10, lines 14-16); and

one or more data processing register values corresponding to data values held within at least some general purpose data processing registers of said apparatus (col 10, lines 35-55).

14. As per claim 3, Ishimoto teaches wherein said processing being performed when said first interrupt event occurred was one of (col 4 lines 4-14):

execution of an active interrupt handling program, said interrupt controller being a nested interrupt controller permitting a pending interrupt handling program to pre-empt said active interrupt handling program if said active interrupt handling program has a lower priority than said pending interrupt handling program (fig 1,element 1; col 1, lines 31-40; col 7, lines 60-63; col 10 lines 25-28).

Ishimoto does not disclose specifically the processing being the execution of a non-interrupt triggered program.

However, Miu teaches that execution of a non-interrupt triggered program (col 3, lines 60-66).

15. As per claim 4, Ishimoto teaches, wherein said first interrupt event and said one or more second interrupt events each have respective priority values, said interrupt controller being operable to compare said respective priority values to determine if any of said one or second interrupts event has a higher priority than said first interrupt event and if so to pre-empt execution of said first interrupt handling program with execution of said a second interrupt handling program (col 4, lines 65-68; col 5, lines 1-19).

16. As per claim 5, Ishimoto teaches wherein said respective priority values are programmable values (col 4, lines 61-64).

17. As per claim 6, Ishimoto teaches wherein said interrupt controller is responsive to a late interrupt signal during reloading of said first state data to abort a return to said processing being performed when said first interrupt event occurred and instead redirect execution to an interrupt handling program associated with said late interrupt signal (col 9, lines 5-22).

18. As per claim 7, Ishimoto teaches wherein if such a said second interrupt event has occurred, then redirection of program instruction execution to said second interrupt handling

program occurs without reloading said first state data from said stack data store (col 9, lines 5-55).

19. As per claim 10, Miu teaches wherein transfer of data values to said stack data store under control of said interrupt controller is performed in parallel with and asynchronously to loading of program counter location and program instructions into an instruction pipeline prior to execution (col 10, lines 35-43).

20. As per claim 11, Miu teaches, wherein said interrupt controller is responsive to execution of a return instruction with a predetermined link address value loaded within a link register to perform a return from interrupt operation (col 2, lines 54-59).

21. As per claim 12, Ishimoto teaches wherein said stack data store is a stack memory (col 7, lines 37-41).

22. As per claims 14-20 and 23-25, they are method claims of claim 1-7 and 10-12 above. Therefore, they are rejected under the same rational as claim 1-7 and 10-12 above.

23. Claims 8, 9, 21 and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Miu et al.(Miu) US Patent No. 4,488,227, in view of Ishimoto et al.(Ishimoto) US Patent No. 5,410,715, and further in view of McMahan.(McMahan) US Patent No. 5,706,491.

24. As per claim 8, the combined method of Miu and Ishimoto does not specifically disclose repairing to undo any partial return call.

25. However, McMahan teaches wherein upon aborting said return, said stack data store is repaired to undo any alterations made by partial completion of said return (col 3, lines 54-67; col 4, lines 1-20).

26. Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of McMahan into the combined method of Ishimoto and Miu for repairing any unsuccessful return. The modification would have been obvious because one of the ordinary skills of the art would want to repair the unsuccessful return for future execution of unfinished processes.

27. As per claim 9, McMahan teaches wherein said repair includes repairing one or more of stack pointer data and link register data (col 4, lines 4-20).

28. As per claims 21 and 22, they are method claims of claim 8 and 9 above. Therefore, they are rejected under the same rational as claim 8 and 9 above.

29. Claims 13 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Miu et al.(Miu) US Patent No. 4,488,227, in view of Ishimoto et al.(Ishimoto) US Patent No. 5,410,715, and further in view of Raasch et al.(Raasch) US Patent No. 5,237,692.

30. As per claim 13, the combined method of Miu and Ishimoto does not specifically disclose of entering a low power mode when no pending interrupt is available.

31. However, Raasch teaches wherein when there are no pending interrupts said apparatus enters a low power mode in which processing is halted awaiting an interrupt event (col 2, lines 63-68; col 3, lines 1-4).

32. Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Raasch into the combined method of Ishimoto and Miu for entering a low power mode when no interrupt to process. The modification would have been obvious because one of the ordinary skills of the art would want to enter a low power mode to conserve power and system resources.

33. As per claim 26, it is a method claim of claim 13 above. Therefore, it is rejected under the same rational as claim 13 above.

Response to Arguments

34. Applicant's arguments filed 10/01/2008 have been fully considered but they are not persuasive.

35. In the remarks applicant argues:

(1) Ishimoto fails to teach having a stack priority level corresponding to the highest priority interrupt among the stacked interrupts.

36. Examiner respectfully disagree to applicant:

i. As to point (1), applicant supports his argument with mentioning that Ishimoto teaches having an in service priority which is the highest priority that is being serviced and fails to teach id the priority levels of the stacked priority can be altered then the priority of the top of the stack can be changed. Examiner respectfully disagrees with the applicant. The claim limitation is not clear and does not disclose altering the priority of the stack when an interrupt is in service which can make an interrupt higher than the interrupt in service or the interrupt stored in top of the stack. The claim limitation recites having only one process state being saved in the stack and does not specify that any other interrupted process or interrupt events are pre-empted in the stack than the process that was interrupted to service the first interrupt or any other interrupt event. Moreover the determination is being done or checked once the interrupted process has already been reloaded after completing the first interrupt that means the interrupt in service are never pre-empted and there are no more data left in the stack to determine the stack priority level, even if the determination was done before the interrupted process was reloaded still the priority of the process will be the priority of the stack as that is the only state data stored in the stack. According the examiner interprets the stack priority level as the process or interrupt in service or the process that was interrupted when the first interrupt service is complete.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VAN H NGUYEN/
Primary Examiner, Art Unit 2194

/Abdullah-Al Kawsar/
Examiner, Art Unit 2195